ANALYSIS AND SIMULATION OF MANUFACTURED SCREEN-PRINTED SOLAR CELLS

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ABSTRACT

A detailed study has been conducted of the performance of millions of screen-printed solar cells to analyse the various processing parameters and their interdependencies. Algorithms have been developed to quite accurately predict device structure and hence performance as a function of the many manufacturing processing parameters. The processes characterized include the saw-damage removal etch, anisotropic texturing, emitter diffusion, edge junction isolation, AR coating deposition and the screen-printing and firing of the front and rear metal contacts. From the developed algorithms, a simulator has been developed which includes the natural variations in device parameters that occur in a real production environment due to relatively random effects such as thermal gradients within furnaces, slight fluctuations in belt speeds, gas flows, plasma etching power, chemical concentrations, furnace temperature controllers, wafer quality, etc,. These can have a significant effect on electrical yields. Even common factors affecting the mechanical yields in production have been programmed into the simulator. Since the virtual production line was primarily developed for the purposes of educating and training engineers, extensive in-line quality control testing has also been incorporated, such as the measurement of: minority carrier lifetimes; substrate resistivity; emitter sheet resistivity; wafer thickness; screen-printing paste thickness and width; AR coating thickness and refractive index; surface reflection; spectral response; I-V characteristics; series resistance; shunt resistance; ideality factor; doping profile; etc.

BACKGROUND

The photovoltaic(PV) industry continues to rapidly expand, with 1million jobs expected to be created by 2020 [1,2].

Screen-printed solar cell technology based on the use of multi or mono-crystalline silicon substrates, dominates the commercial production of solar cells. Although many of the screen-printed solar cell processes are common between manufacturers, exceptions include:
Czochralski versus multicrystalline silicon wafers; Textured surfaces versus planar surfaces; AR coatings versus no AR coating; Co-fired metal contacts versus separately fired contacts; Fire-through versus non-fired-through metal contacts; SiN versus TiO2 AR coating; Tube diffusion versus belt diffusion; Plasma-etched versus laser edge-junction isolation; Al versus Al doped silver for rear metal.

SIMULATION OF THE MANUFACTURING OF SCREEN_PRINTED SOLAR CELLS

A virtual production line (VPL) for the manufacturing of screen-printed solar cells has been developed to simulate the production environment and corresponding production processes and results. It was developed so as to be an educational tool for the training of engineers. Operators of the VPL can in general choose between the various options/variations described above. Many manufacturers are now opting for fire-through metal contacts whereby the AR coating is deposited at relatively low temperatures prior to the front surface metallisation so as to facilitate subsequent penetration of the silver through the layer when heated to produce ohmic contact to the silicon.

Another popular simplification is the co-firing of the two metal contacts whereby the aluminium rear and the silver front contacts are sequentially printed then dried prior to the co-firing of both metal contacts in a single high temperature step. Simplicity is one obvious benefit of this co-firing with the removal of one high temperature process. Another benefit, however, is the improved mechanical yields through avoiding the reasonably severe stressing and bowing of the wafer that accompanies the formation of the rear aluminium contact independently of the front contact. The disadvantage however of co-firing is that the optimised firing conditions for the rear contact are often quite different from those required for the front contact.

CRYSTALLOGRAPHIC TEXTURING

Texturing of crystalline silicon wafers is commonly used to produce surface pyramids as shown in figure 1. These pyramids greatly reduce surface reflection and are formed by etching the silicon surface with a weak anisotropic etch such as dilute sodium hydroxide which etches the high density <111> planes of silicon significantly more slowly than the other planes. When such an etch is used in conjunction with crystalline silicon, the slower etching <111> planes will be exposed at the surface in a configuration dependent on the orientation of the silicon crystal. For wafers that are of (100) orientation, the exposed <111> planes will intersect so as to form upright tetrahedral pyramids on the wafer surface as shown.

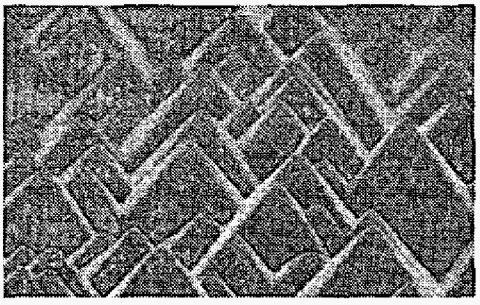

Figure 1: Textured silicon through weak NaOH etching

A detailed study of the texturing process has been conducted in the manufacturing environment using standard commercial infrastructure and equipment. One of the main challenges in producing good quality texturing lies with the tendency for the dilute sodium hydroxide solution to etch the peaks of the pyramids. This will gradually destroy existing pyramids with the final quality of the textured surface dependent upon the relative rates of new pyramid nucleation versus existing pyramid destruction.

The most common approach used to minimize the destruction of existing pyramids is to add isopropanol to the texturing solution. It appears that carbon precipitates in the texturing solution originating from the isopropanol adhere to the silicon surface thereby preventing etching at that point. This nucleates the growth of a pyramid whereby its apex is protected from being etched by the presence of the carbon precipitate. Provided a high density of these precipitates can be retained on the silicon surface for approximately 15-20 minutes, good quality texturing can be achieved. Good quality refers to the uniformity of the pyramid distribution, the achievement of pyramid dimensions in the range of 3-10 microns (across the pyramid base), 100% coverage of the wafer surface with pyramids, and pyramid bases that are not rounded but rather are formed through the sharp intersection between adjacent <111> planes.

The most commonly used formula for texturing is to use 2% W/V sodium hydroxide at 90-95°C with approximately 5% (by volume) propanol added immediately prior to immersing the wafers in the texturing solution. Repeated use of the same texturing solution is essential in manufacturing environments, with residual quantities of isopropanol remaining from the previous batch of texturing. Critical parameters that have been found to have an impact on the quality of the texturing include: isopropanol concentration; sodium hydroxide concentration; temperature of the solution; evaporation rate of isoproponal from the solution surface which is dependent on exhausting arrangements and the type of cover used; time delay between batches; wafer's surface finish prior to texturing; duration of the texturing process; accumulation of sodium silicate within the texturing batch; and the number of wafers included in each batch.

The best texturing quality was achieved after the solution had been used to texture about 1,000 wafers. At this stage, the initial addition of 5% propanol per batch was reduced to about 1-2% per batch as the sodium silicate concentration in the solution increased, thereby reducing the importance of the propanol. The high propanol concentration for early batches was found to be necessary for adequate density of pyramid nucleation, while a very high exhaust rate was found beneficial to rapidly reduce the propanol concentration during texturing, apparently to prevent further pyramid nucleation late in the process that potentially destroys existing pyramids. The solution was nominally 2% W/V sodium hydroxide solution heated to approximately 90°C. The isopropanol was gradually added over a period of about 30 seconds. The wafers will then be gently immersed in the solution for a period of 15-20 minutes. The length of time required for the texturing process depends very much on the size of pyramids being formed and their density. The density of the pyramids appears to depend heavily not only on the propanol concentration but also on the type of surface finish the wafer has following the saw damage removal etch. With a high density of pyramid formation, each pyramid only needs to grow to a few microns in size before adjacent pyramids impinge on each other. To grow pyramids of this size, less than 10 minutes of texturing are required

Another important finding has been that once the sodium silicate concentration is sufficiently high to facilitate reduced dependence on isopropanol, greater variation in many of the other processing parameters can then be tolerated such as exhaust rate, time between batches, solution turbulence, wafer surface finish prior to texturing, number of wafers being textured, and even the solution temperature. To avoid the poorer reliability of the texturing for the first 1,000 wafers textured in a new solution, each new solution can instead be made up by retaining half of the old solution with its high sodium silicate concentration and adding to it an equal volume of new solution. In this case, the propanol addition per batch need only be about 2% initially, reducing to less than 1% per batch after several uses of the solution.

All of these parameters and interdependencies have been incorporated into the VPL in accordance with data generated on real production lines. Despite the attempts to accurately model these processes, the complexities and parameter interactions make it difficult to guarantee the accuracy of the predicted texturing quality. To improve the usefulness of the VPL as an educational tool, extensive notes have been provided that accompany each process with a detailed explanation of the impact of each parameter and the various parameter interdependencies.

EMITTER FORMATION

The phosphorus diffusion is perhaps the most critical process in determining the performance of screen printed solar cells. On the one hand, a very heavily diffused emitter with a deep junction will create a dead layer near the surface that will result in poor performance to short wavelength light. At the other extreme, if the emitter is diffused too lightly or if the junction is too shallow, problems result in making a good ohmic contact between the silver and the n-type silicon. This occurs because the contact resistance is strongly dependent on the phosphorus concentration at the interface between the silver and the silicon and also because the silver penetrates a significant distance into the n-type silicon which will therefore cause problems if the junction is too shallow. The lightly diffused emitter will also lead to high lateral resistive losses due to the widely spaced screen-printed metal fingers that are typically 3mm apart.

These factors have all been incorporated into the VPL with the time and temperature of the diffusion process having a significant impact on the resulting junction depth and sheet resistivity. Phosphorus gettering, particularly with multicrystalline silicon wafers, has also been included within the modelled performance of the devices. Diffusion down the edges of the wafers has been included along with the corresponding shunting of the devices in the absence of appropriate edge junction isolation. The most common approach for edge isolation is to use plasma etching of the edges following coin stacking of the wafers. This process is relatively straight forward with the main user specified parameters being the power for the plasma, the duration of the process and the gas composition. Etching of the edges, however, using a plasma creates some damage to the surface of silicon. Some of this damage penetrates into the junction causing the device ideality factor to rise. High powered plasmas are useful for high throughput but create more damage. Users of the VPL specify the diffusion temperature, the belt speed for the furnace (and hence the diffusion time), the properties of the diffusion source and the desired edge junction isolation parameters.

ALUMINIUM PRINTED REAR CONTACT

Wafers periodically break during the firing of the aluminium paste. The probability of a wafer breaking is also increased if "pimpling" or roughening of the rear metal contact occurs due to either lack of oxygen in the firing furnace or inadequately dried aluminium paste prior to the wafers entering the high temperature section. Lack of oxygen in the ambient prevents the formation of an adequately thick aluminium oxide layer across the rear of the aluminium layer. At temperatures above 577°C, aluminium/silicon material in intimate contact with each other melts. Once the temperature is above 650°C, all of the aluminium melts with the resulting rear molten layer requiring the overlying aluminium oxide layer to prevent surface tension and other effects from causing "balling up" of the molten material. Any tendency to produce a rough rear surface will lead to greater stressing of the wafer and much greater probability of breakage during subsequent processing when wafers are placed on a surface with a wafer hold-down mechanism. Wafer breakage during aluminium printing, drying or firing can be of major importance if aluminium paste subsequently contaminates belts or transfer mechanisms. This is because wafers are processed face down such that any contamination of the surfaces could lead to small amounts of aluminium being transferred to the front surfaces of subsequent wafers, therefore causing shunting of the phosphorus diffused junction during the high temperature process. In attempting to realistically reproduce the production environment, all of these factors have been incorporated into the VPL with wafers having a finite probability of breakage that depends on the wafer thickness, aluminium paste thickness, firing conditions, etc.. Yields are also an extremely important figure of merit for all production lines, with the VPL placing similar importance on the yields on each processing step and the process as a whole.

AR COATING & SILVER FRONT CONTACT

The obvious immediate benefit of the AR coating is through the improved optical performance of the solar cells through reducing reflection from the surface, particularly for multicrystalline silicon wafers that cannot be easily textured. For the latter, plasma enhanced chemical vapour deposition of silicon nitride is the preferred option due to the generation of atomic hydrogen that is important for grain boundary passivation. The thickness is determined by the duration of the process and the gas flow rate. The temperature of deposition can also be a very important parameter if fire-through metal contacts are being used. The latter refers to the screen printing of the silver metal paste on top of the AR coating layer with the subsequent metal firing process being used to drive the silver through the AR coating into the surface of the silicon. Provided the process is well controlled, the fire through contacts can be used to prevent the silver from penetrating as far into the silicon as would otherwise be the case. This can allow shallower junctions to be used and therefore higher sheet resistivities for the emitter with corresponding reduced dead layers as previously discussed. Clearly, the uniformity of the AR coating thickness across the wafer surface becomes an important parameter in determining the effectiveness of the fire-through process. Similarly, the temperature of the deposition determines the hardness of the AR coating layer and therefore the resistance it provides to the metal penetration. Well controlled processes can facilitate significant improvements in the performance of screen printed devices although poor parameter control can lead to significant numbers of wafers failing either because metal has penetrated through to the junction in localised regions or else metal fails to penetrate right through the AR coating to make contact to the silicon. These interdependencies and parameter variations have been programmed into the VPL.

IN-LINE QUALITY CONTROL

An important aspect of the education/training of engineers for this manufacturing environment involves the gaining of expertise in the techniques and methods available for the testing and analysis of partially processed solar cells. The VPL therefore incorporates all known in-line quality control tests and techniques that are used on production lines throughout the world. Understanding the importance of these tests and gaining expertise in their use is recognised as one of the most important educational functions able to be performed through the VPL.

The in-line tests available to the user of the VPL include analysis of minority carrier lifetimes, wafer thickness/resistivity, surface reflection as a function of wavelength, quality of texturing, thicknesses of printed pastes, series and shunt resistances, complete current-voltage output characteristics, spectral response, metal resistive losses, doping profiles, etc.. In addition, quality control procedures implemented on the VPL specifically train students/engineers in how to most effectively use all of these tests to quickly and efficiently identify problems at any point within the production sequence.

PRODUCTION YIELDS

It is unavoidable that many of the manufacturing processing parameters vary slightly and therefore may affect yields. For example, temperature gradients within chemical solutions, slight fluctuations in furnace temperatures, slight variations in wafer thicknesses, etc. are parameters that cannot be controlled precisely. Processes must therefore be sufficiently robust to the achievable tolerances in the processing parameters to avoid unacceptable loss in device performance. This inevitably necessitates some compromise between device performance and device yields. For example, the highest performance devices can be achieved with shallow heavily diffused emitters with screen printed silver contacts that only penetrate a very small distance into the silicon. This, in theory, can be achieved in conjunction with the use of an AR coating of precise thickness and hardness and the use of precise firing conditions for the screen printed silver. For such high performance devices, a slight increase in the depth of metal penetration will lead to puncturing of the junction and/or increased contact resistance while insufficient metal penetration can lead to the inability to make ohmic contact to the n-type region. In such a finely tuned process, slight variation in the AR coating thickness or its hardness or the metal firing temperature can lead to one or other of these extremes being reached with subsequent electrical failure of the device. The issue of yields is therefore of considerable importance and has accordingly been incorporated into the VPL with the aim of realistically representing true production environments.

EXAMPLES OF RESULTS FROM THE VPL

Based on large volumes of data generated on real production lines, algorithms have been developed to simulate device performance as a function of processing parameters selected for the VPL. In conjunction with this, the 1-dimensional numerical modelling package PC-1D [3] has been adapted for use within the VPL for doing some of the device optical and electrical analysis. The accuracy of the simulated solar cell results from the VPL have been shown to closely approximate those produced in the real production environment provided the processing parameters are not too extreme. Figure

2 shows the surface reflection analysis for a CZ wafer following texturing on the VPL.

In comparison, Figure 3 shows the impact of using the VPL to apply an AR coating of close to optimal thickness and refractive index. Here the reflection at the minima of the curve is amost zero due to the absence of the front metal contact which would otherwise normally reflect 10-15% of incoming light across the spectrum.

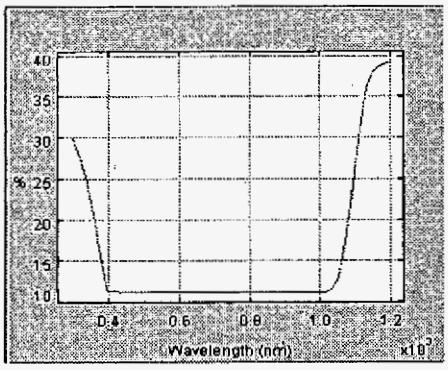

Figure 2: Reflection curve for a VPL textured CZ wafer

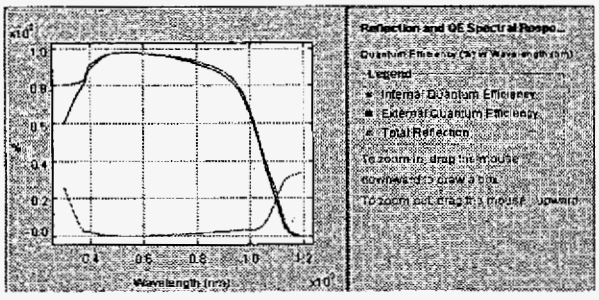

Figure 3: Rreflection curve (lower) for a textured and AR coated silicon wafer fabricated on the VPL. The upper curves represent the IQE and EQE for the same wafer prior to applying the front metal contact.

At the completion of the diffusion process on the VPL, the sheet resistivity and doping profile can be determined with the latter shown in Figure 4. This profile is a function of the diffusion processing conditions used for the VPL such as the time and temperature and the diffusion source type.

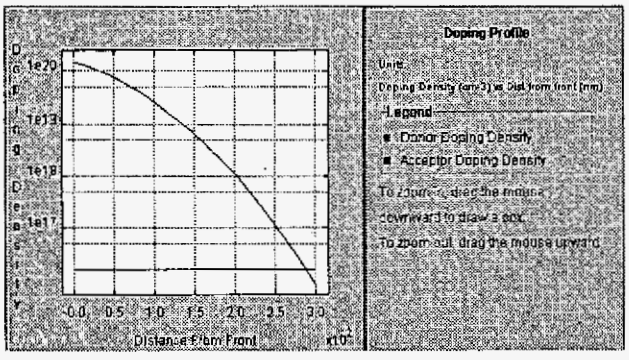

Figure 4: Doping profile of a VPL diffused wafer.

The analysis of the spectral response of cells fabricated on the VPL gives considerable insight into the strengths and weaknesses of the device and the recombination processes throughout. This test can be applied at any point following the diffusion as shown in Figure 2. However, the external quantum efficiency curve probably only has significance following the front surface metallisation when the reflection from the metal is included.

Cells fabricated on the VPL are automatically tested on completion under standard test conditions to determine their current-voltage characteristics. An example of this analysis for a screen-printed cell produced on the VPL is shown in Figure 5. As typical of most screen-printed cells, this cell has a poor blue response due to the surface dead layer caused by the heavy phosphorus diffusion and a poor fill-factor resulting from high series resistance associated with the front metallisation. This cell however has a lower than normal Voc resulting from the high substrate resistivity used and also a lower than normal Jsc as a result of a higher than optimal metal shading loss in the vicinity of 20%.

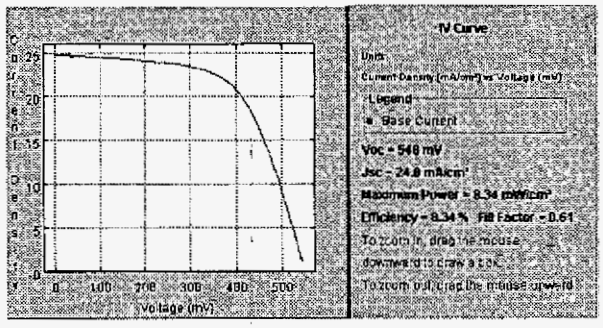

Figure 5 Typical IV curve for a screen-printed solar cell manufactured on the VPL with non-optimal processing parameters.

CONCLUSIONS

A virtual production line (VPL) for solar cell manufacturing has been developed and evaluated. It is based on algorithms formulated from the data and analysis of large numbers of commercial screen-printed solar cells, and appears to quite accurately predict device performance. The VPL has proven to be an effective tool in the training and teaching of engineers. It facilitates process optimisation and in-line quality control testing. Strong support has been provided by industry and the Australian Government in the development of the VPL.

ACKNOWLEDGEMENTS

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